REMARKS

The enclosed is responsive to the Examiner's Office Action mailed on October 13, 2005.

At the time the examiner mailed the Office Action claims 26-31 and 34-39 were pending. By way of the present response the Applicant has 1) canceled claims 26-31 and 34-39; 2) added new claims 58-69; and 3) argued that newly added independent claims 58 and 64 are patentable over cited references. The Applicant respectfully requests reconsideration of the present application and the allowance of all claims as presented.

The Applicant has canceled claims 26-31 and 34-39 rendering moot the Examiner's rejections in the Office Action mailed on October 13, 2005.

NEWLY ADDED INDEPENDENT CLAIMS

Newly added independent claims 58 and 64 presently recite (emphasis added):

58. (new) A method comprising:
searching a semiconductor device design to find a found carry chain, a logical function implemented with said found carry chain;
calculating a first propagation delay through said found carry chain;
splitting said found carry chain into two or more carry chains;
connecting said two or more carry chains in parallel to form a parallel carry chain having same inputs and outputs as said found carry chain;
calculating a second propagation delay through said parallel carry chain; and
modifying said semiconductor device design by replacing said found carry chain with said parallel carry chain if said second propagation delay is smaller than said first propagation delay.

64. (new) A machine readable medium having stored thereon sequences of instructions which are executable by a digital processing system, and which, when executed by the digital processing system, cause the system to perform a method comprising:
searching a semiconductor device design to find a found carry chain, a logical function implemented with said found carry chain;
calculating a first propagation delay through said found carry chain;
splitting said found carry chain into two or more carry chains;
connecting said two or more carry chains in parallel to form a parallel carry chain having same inputs and outputs as said found carry chain;
calculating a second propagation delay through said parallel carry chain; and
modifying said semiconductor device design by replacing said found carry chain with said parallel carry chain if said second propagation delay is smaller than said first propagation delay.

The Examiner applied one reference, US Patent 6,359,468 (hereinafter "Park") in rejecting previously submitted independent claims 26 and 34.

Newly added independent claims 58 and 64 are directed to searching a semiconductor device design to find a found carry chain, a logical function implemented with the found carry chain, splitting the found carry chain into two or

more carry chains, connecting the two or more carry chains in parallel to form a parallel carry chain having same inputs and outputs as said found carry chain, and modifying the semiconductor device design by replacing the found carry chain with the parallel carry chain if the second propagation delay is smaller than the first propagation delay. The claims are supported by the Applicant's specification. To be specific, the terms "second propagation delay is smaller than said first propagation delay" and "replacing a single carry chain with parallel carry chains" are supported by the Applicant's specification on page 9 line 18 through page 10 line 2. Figure 2A and 2B of the Applicant's specification shows that the parallel carry chain implementation derived by combining elements 201a and 201b has the same inputs and outputs as in a single carry chain.

Park discloses predicting or determining the values of carry signals. However, Park does not searching a semiconductor device design to find a found carry chain, a logical function implemented with the found carry chain. Park discloses two carry out signals and selecting the faster one to reduce the propagation delay. However, Park does not teach, disclose, or suggest splitting the found carry chain into two or more carry chains and connecting the two or more carry chains in parallel to form a parallel carry chain having same inputs and outputs as the found carry chain. Park is silent as to making any modification in the semiconductor device design to select a faster carry out signal. Therefore, Park does not teach, disclose, or suggest modifying the semiconductor device design by replacing the found carry chain with the parallel carry chain if the second propagation delay is smaller than the first propagation delay.

Therefore, Park fails to disclose, teach, or suggest searching a semiconductor device design to find a found carry chain, a logical function implemented with the found carry chain, splitting the found carry chain into two or more carry chains, connecting the two or more carry chains in parallel to form a parallel carry chain having same inputs and outputs as the found carry chain, and modifying the semiconductor device design by replacing the found carry chain with the parallel carry chain if the second propagation delay is smaller than the first propagation delay.

Therefore, the applicant's independent claims 58 and 64 are patentable over the Park reference. Because each of the Applicant's independent claims are patentable, the Applicant respectfully submits that all of the Applicant's claims are patentable, and, respectfully request the allowance of same.

CONCLUSION

Applicant respectfully submits that all rejections have been overcome and that all pending claims are in condition for allowance.

If there are any additional charges, please charge them to our Deposit Account Number 02-2666. If a telephone conference would facilitate the prosecution of this application, the Examiner is invited to contact James Scheller at (408) 720-8300.

Respectfully Submitted,

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